CLAIMS:

1. A test wrapper architecture for testing an electronic circuit having one or more hierarchical cores, the test wrapper architecture comprising:

- a first core having a wrapper input cell and a wrapper output cell, the wrapper input cell and wrapper output cell being configured to receive a primary input signal and a test input signal for the first core, and to output a primary output signal and a test output signal for the first core;

- a second core having a wrapper input cell and a wrapper output cell, the wrapper input cell and wrapper output cell being configured to receive a primary input signal and a test input signal for the second core, and to output a primary output signal and a test output signal for the second core;

wherein the wrapper input cell and the wrapper output cell of the second core are further adapted to receive a test input signal from the first core, and to output a test output signal to the first core, thereby enabling the first core and the second core to be tested in parallel.

2. A test wrapper architecture as claimed in claim 1, wherein the wrapper input cell and wrapper output cell of the second core are adapted to operate in a In-test mode and an Ex-test mode in parallel.

3. A test wrapper architecture as claimed in claim 2, wherein the wrapper input cell and wrapper output cell of the second core are adapted to apply and capture data in parallel.

4. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper input cell of the second core is adapted to connect the test input signal of the second core to the test output signal of the second core in a first mode of operation.

5. A test wrapper architecture as claimed in claim 4, wherein the first mode of operation corresponds to a In-test shift mode, during which test data is being shifted through the wrapper input cell via a first memory means.

6. A test wrapper architecture as claimed in claim 5, wherein the wrapper input cell is adapted to connect the data stored in the first memory means to the primary output signal in a second mode of operation.

7. A test wrapper architecture as claimed in claim 6, wherein the second mode of operation corresponds to a In-test normal mode, during which the test data stored in the first memory means during a previous shift operation is connected to the primary output of the wrapper input cell.

8. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper input cell of the second core is adapted to connect the test input signal of the first core to the test output signal of the first core in a third mode of operation, via a second memory means.

9. A test wrapper architecture as claimed in claim 8, wherein the third mode of operation corresponds to a Ex-test shift mode, during which test data is shifted between the test input and the test output via the second memory means.

10. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper input cell of the second core is adapted to connect the primary input signal of the second core to the second memory means in a fourth mode of operation.

11. A test wrapper architecture as claimed in claim 10, wherein the fourth mode of operation corresponds to a Ex-test normal mode, during which test response data received from the primary input of the first core is stored in the second memory means.

12. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper output cell of the second core is adapted to connect the test input signal of the second core to the test output signal of the second core in a first mode of operation.

13. A test wrapper architecture as claimed in claim 12, wherein the first mode of operation corresponds to a In-test shift mode, during which test data is being shifted through the wrapper output cell via a third memory means.

14. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper output cell of the second core is adapted to connect the primary input signal to the third memory means in a second mode of operation.

15. A test wrapper architecture as claimed in claim 14, wherein the second mode of operation corresponds to a In-test normal mode, during which the test response data observed from the second core is stored in the third memory means.

16. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper output cell of the second core is adapted to connect the test input signal of the first core to the test output signal of the first core in a third mode of operation, via a fourth memory means.

17. A test wrapper architecture as claimed in claim 16, wherein the third mode of operation corresponds to a Ex-test shift mode, during which test data is shifted between the test input and the test output via the fourth memory means.

18. A test wrapper architecture as claimed in claim 2 or 3, wherein the wrapper output cell of the second core is adapted to connect test data stored in the fourth memory means to the primary output for the first core in a fourth mode of operation.

19. A test wrapper architecture as claimed in claim 18, wherein the fourth mode of operation corresponds to a Ex-test normal mode, during which test data stored in the fourth memory is connected to the primary output for the first core.

20. A test wrapper architecture as claimed in any one of claims 5, 8, 13 or 16, wherein one or more of the memory means is a flip-flop.

21. A test wrapper architecture as claimed in any one of the preceding claims, wherein the first core is a parent core and the second core is a child core in the hierarchy.

22. A wrapper cell for a test architecture used for testing an electronic circuit having one or more hierarchical cores, the wrapper cell comprising:

- a first input for receiving a primary data signal;
- a second input for receiving a test data signal;

- a first output for outputting a primary data signal;

a second output for outputting a test data signal;

wherein the wrapper cell further comprises a third input for receiving a test input signal from another core, and a third output for outputting a test output signal to the other core.

23. A wrapper cell as claimed in claim 22, wherein the wrapper cell is an input wrapper cell comprising:

- a first multiplexer, the first multiplexer having a first input connected to the first input signal, a second input connected to an output of a first memory means and to the second output of the wrapper cell, and having an output connected to the first output of the wrapper cell;
- a second multiplexer, the second multiplexer having a first input connected to the second input of the wrapper cell, a second input connected to the first output of the wrapper cell, and having an output connected to the input of the first memory means; and
- a third multiplexer, the third multiplexer having a first input connected to the first input of the wrapper cell, a second input connected to the third input of the wrapper cell, and an output connected to the third output of the wrapper cell via a second memory means.

24. A wrapper input cell as claimed in claim 23, wherein in a first mode of operation (In-test shift) the wrapper input cell is adapted to connect the second input to the second output, via the first memory means.

25. A wrapper input cell as claimed in claim 23, wherein in a second mode of operation (In-test normal), the wrapper input cell is adapted to output data stored in the first memory means to the first output.

26. A wrapper input cell as claimed in claim 23, wherein in a third mode of operation (Ex-test shift), the wrapper input cell is adapted to connect the third input to the third output via the second memory means.

27. A wrapper input cell as claimed in claim 23, wherein in a fourth mode of operation (Ex-test normal), the wrapper input cell is adapted to connect the first input to the second memory means.

28. A wrapper cell as claimed in claim 22, wherein the wrapper cell is an output wrapper cell comprising:

- a first multiplexer, the first multiplexer having a first input connected to the first input signal, a second input connected to an output of a first memory means and to the third output of the wrapper output cell, and having an output connected to the first output of the wrapper output cell;
- a second multiplexer, the second multiplexer having a first input connected to the second input of the wrapper output cell, a second input connected to the first input of the wrapper output cell, and having an output connected to the input of a second memory means; and
- a third multiplexer, the third multiplexer having a first input connected to the first input of the wrapper output cell, a second input connected to the third input of the wrapper output cell, and an output connected to the third output of the wrapper output cell via the first memory means.

29. A wrapper output cell as claimed in claim 28, wherein in a first mode of operation (In-test shift) the wrapper output cell is adapted to connect the second input to the second output, via the second memory means.

30. A wrapper output cell as claimed in claim 28, wherein in a second mode of operation (In-test normal), the wrapper output cell is adapted to connect the first input to the second memory means.

31. A wrapper output cell as claimed in claim 28, wherein in a third mode of operation (Ex-test shift), the wrapper output cell is adapted to connect the third input to the third output via the first memory means.

32. A wrapper output cell as claimed in claim 28, wherein in a fourth mode of operation (Ex-test normal), the wrapper output cell is adapted to connect test data stored in the first memory means to the first output.

33. A wrapper output cell as claimed in any one of claims 28 to 32, further comprising a fourth multiplexer having a first input connected to receive the output of the

third multiplexer and a second input connected to receive the output of the first multiplexer, the output of the fourth multiplexer providing the input to the first memory means.

34. A wrapper output cell as claimed in claim 33, wherein the wrapper output cell is adapted to test the third multiplexer.

35. A method of testing an electronic circuit having one or more hierarchical cores, the method comprising the steps of:

- in a first core having a wrapper input cell and a wrapper output cell, configuring the wrapper input cell and wrapper output cell to receive a primary input signal and a test input signal for the first core, and to output a primary output signal and a test output signal for the first core;
- in a second core having a wrapper input cell and a wrapper output cell, configuring the wrapper input cell and wrapper output cell to receive a primary input signal and a test input signal for the second core, and to output a primary output signal and a test output signal for the second core; and
- configuring the wrapper input cell and the wrapper output cell of the second core to receive a test input signal from the first core, and to output a test output signal to the first core, thereby enabling the first core and the second core to be tested in parallel.

36. An integrated circuit comprising a test wrapper architecture as claimed in claims 1 to 21 or a wrapper cell as claimed in claims 22 to 34.

37. An automatic test equipment comprising means for operating a test wrapper architecture as defined in claims 1 to 21, or a wrapper cell as claimed in claims 22 to 34.